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(54) Title: NITRIDE-BASED TRANSISTORS AND METHODS OF FABRICATION THEREOF USING NON-ETCHED CONTACT RECESSES

(57) Abstract: Contacts for a nitride based transistor and methods of fabricating such contacts provide a recess through a regrowth process. The contacts are formed in the recess. The regrowth process includes fabricating a first cap layer comprising a Group III-nitride semiconductor material. A mask is fabricated and patterned on the first cap layer. The pattern of the mask corresponds to the pattern of the recesses for the contacts. A second cap layer comprising a Group III-nitride semiconductor material is selectively fabricated (e.g. grown) on the first cap layer utilizing the patterned mask. Additional layers may also be formed on the second cap layer. The mask may be removed to provide recess(es) to the first cap layer, and contact(s) may be formed in the recess(es). Alternatively, the mask may comprise a conductive material upon which a contact may be formed, and may not require removal.

NITRIDE-BASED TRANSISTORS AND METHODS OF FABRICATION THEREOF USING NON-ETCHED CONTACT RECESSES

RELATED APPLICATION

The present application claims the benefit of United States Provisional Application Serial No. 60/396,236 (Attorney Docket No: 5308-248PR), filed July 16, 2002, the disclosure of which is hereby incorporated by reference in its entirety.

FIELD OF THE INVENTION

The present invention relates to semiconductor devices and, more particularly, to transistors that incorporate nitride-based active layers.

BACKGROUND

The present invention relates to transistors formed of semiconductor materials that can make them suitable for high power, high temperature, and/or high frequency applications. Materials such as silicon (Si) and gallium arsenide (GaAs) have found wide application in semiconductor devices for lower power and (in the case of Si) lower frequency applications. These, more familiar, semiconductor materials may not be well suited for higher power and/or high frequency applications, however, because of their relatively small bandgaps (*e.g.*, 1.12 eV for Si and 1.42 for GaAs at room temperature) and/or relatively small breakdown voltages.

In light of the difficulties presented by Si and GaAs, interest in high power, high temperature and/or high frequency applications and devices has turned to wide bandgap semiconductor materials such as silicon carbide (2.996 eV for alpha SiC at room temperature) and the Group III nitrides (*e.g.*, 3.36 eV for GaN at room temperature). These materials, typically, have higher electric field breakdown strengths and higher electron saturation velocities as compared to gallium arsenide and silicon.

A device of particular interest for high power and/or high frequency applications is the High Electron Mobility Transistor (HEMT), which is also known as a modulation doped field effect transistor (MODFET). These devices may offer

operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. The 2DEG is an accumulation layer in the undoped ("unintentionally doped"), smaller bandgap material and can contain a very high sheet electron concentration in excess of, for example, 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.

This combination of high carrier concentration and high carrier mobility can give the HEMT a very large transconductance and may provide a strong performance advantage over metal-semiconductor field effect transistors (MESFETs) for high-frequency applications.

High electron mobility transistors fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system have the potential to generate large amounts of RF power because of the combination of material characteristics that includes the aforementioned high breakdown fields, their wide bandgaps, large conduction band offset, and/or high saturated electron drift velocity. A major portion of the electrons in the 2DEG is attributed to polarization in the AlGaN. HEMTs in the GaN/AlGaN system have already been demonstrated. U.S. Patents 5,192,987 and 5,296,395 describe AlGaN/GaN HEMT structures and methods of manufacture. U.S. Patent No. 6,316,793, to Sheppard et al., which is commonly assigned and is incorporated herein by reference, describes an HEMT device having a semi-insulating silicon carbide substrate, an aluminum nitride buffer layer on the substrate, an insulating gallium nitride layer on the buffer layer, an aluminum gallium nitride barrier layer on the gallium nitride layer, and a passivation layer on the aluminum gallium nitride active structure.

One issue with the fabrication of nitride-based transistors involves the formation of ohmic contacts for such transistors. Conventionally, ohmic contacts have been formed through reactive ion etching (RIE) recesses for the contacts. However, without strict process control practices, RIE in nitride based materials may suffer from uniformity and reproducibility problems. Such problems could result in difficulty in controlling a fabrication process. Ohmic contacts that are formed without RIE have, typically, used high annealing temperatures (*e.g.* 900 °C). Such high annealing temperatures may damage the materials and/or the device.

SUMMARY OF THE INVENTION

Embodiments of the present invention provide contacts for a nitride based transistor and methods of fabricating such contacts by providing a recess utilizing a regrowth process. The contacts are formed in the recess. The regrowth process includes fabricating a first cap layer comprising a Group III-nitride semiconductor material. A mask is fabricated and patterned on the first cap layer. The pattern of the mask corresponds to the pattern of the recesses for the contacts. A second cap layer comprising a Group III-nitride semiconductor material is selectively fabricated (*e.g.* grown) on the first cap layer utilizing the patterned mask. Additional layers may also be formed on the second cap layer. The mask may be removed to provide recess(es) to the first cap layer, and contact(s) may be formed in the recess(es). Alternatively, the mask may comprise a material (conductive or insulating) upon which a contact may be formed, and may not require removal.

In particular, in some embodiments of the present invention, a nitride-based transistor, e.g., a high electron mobility transistor (HEMT) is fabricated. A nitride-based channel layer is formed on a substrate, with or without a buffer layer. A nitride-based semiconductor first cap layer is formed on the nitride-based channel layer. A mask is formed to cover a first portion of the first cap layer and expose an adjacent second portion of the first cap layer. A nitride-based semiconductor second cap layer is formed on the exposed portion of the first cap layer using the mask, e.g., using an epitaxial growth process constrained by the mask. A recess is formed on the first portion of the first cap layer adjacent the second cap layer, for example, by removing the mask to expose the first cap layer or by using a conductive mask upon which the second cap layer does not form. One of an ohmic contact or a gate contact is formed in the recess, and a corresponding gate contact or ohmic contact is formed on the substrate, for example, on the first cap layer and/or on the second cap layer.

The nitride-based channel layer, the nitride-based semiconductor first cap layer, and the nitride-based semiconductor second cap layer may each include a Group-III nitride layer. For example, the channel layer may have a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, wherein the bandgap of the channel layer is less than the bandgap of the first cap layer. Similarly, the first cap layer may include $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

The mask may be formed by, for example, patterning a mask layer using a lift-off technique or a wet-etch technique. The mask may be formed from, for example, a silicon oxide (SiOx) material, a silicon nitride (SiNx) or an aluminum nitride (AlN) based material.

The second cap layer may include the same material as the first cap layer. For example, the first and second cap layers may include AlGaN, and wherein the first cap layer has a higher concentration of Al than the second cap layer. A combined thickness of the first and second cap layers may be about 25 nm.

An additional layer may be formed on the second cap layer. The additional layer may include, for example, a GaN cap layer, an insulating layer, and/or a compositionally graded transition layer.

In further embodiments of the present invention, a contact for a nitride-based microelectronic device may be provided. A nitride-based semiconductor first layer is formed on a substrate. A mask is formed to cover a first portion of the first layer and expose an adjacent second portion of the first layer. A nitride-based semiconductor second layer is formed on the exposed portion of the first layer using the mask. A recess is formed on the first portion of the first layer adjacent the second layer. A contact is formed in the recess. The first and second layer may comprise respective Group III-nitride layers.

According to additional embodiments of the present invention, a transistor includes a nitride-based channel layer on a semi-insulating substrate, a nitride-based semiconductor first cap layer on the nitride-based channel layer and a grown nitride-based semiconductor second cap layer on the first cap layer. An ohmic contact or a gate contact is disposed directly on the first cap layer, adjacent a sidewall of the grown second cap layer, and a corresponding gate contact or ohmic contact is disposed on the substrate, for example, on the first cap layer and/or the second cap layer. The first and second cap layers may comprise respective Group III-nitride layers.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1E are schematic drawings illustrating fabrication of ohmic contacts in a transistor according to embodiments of the present invention.

Figure 2 is a schematic illustration of a transistor according to embodiments of the present invention.

Figure 3 is a schematic illustration of a transistor according to further embodiments of the present invention.

Figure 4 is a schematic illustration of a transistor having a regrown gate recess according to embodiments of the present invention.

Figure 5 is a schematic illustration of a transistor according to some embodiments of the present invention.

Figure 6 is a schematic illustration of a transistor according to further embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and regions illustrated in the figures are illustrated schematically. Accordingly, the present invention is not limited to the relative size, spacing and alignment illustrated in the accompanying figures. As will also be appreciated by those of skill in the art, references herein to a layer formed "on" a substrate or other layer may refer to the layer formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer. It will also be appreciated by those of skill in the art that references to a structure or feature that is disposed "adjacent" another feature may have portions that overlap or underlie the adjacent feature.

Embodiments of the present invention may provide contacts for a nitride-based device through a regrowth process that provides recesses for formation of the contacts through a thin cap layer. By providing recesses for the contacts, reduced anneal temperatures may be used or an anneal may be avoided. Additionally, lower contact resistances may be achieved. Furthermore, by using a regrowth process RIE may also be avoided. Thus, certain embodiments of the present invention may provide improved reproducibility and uniformity. Furthermore, because of the selective area growth of layers, higher strain layers may be provided without cracking.

Embodiments of the present invention may be particularly well suited for use in nitride-based HEMTs such as Group III-nitride based devices. As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds such as AlGaN and AlInGaN. As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (*e.g.*, GaN), ternary (*e.g.*, AlGaN, AlInN), and quaternary (*e.g.*, AlInGaN) compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the Group III elements. Accordingly, formulas such as $Al_xGa_{1-x}N$ where $0 \leq x \leq 1$ are often used to describe them.

Suitable structures for GaN-based HEMTs that may utilize embodiments of the present invention are described, for example, in commonly assigned U.S. Patent 6,316,793 and U.S. application serial no. 09/904,333 filed July 12, 2001 for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," U.S. provisional application serial no. 60/290,195 filed May 11, 2001 for "GROUP III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" and United States Patent Application Serial No. 10/102,272, to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosures of which are hereby incorporated herein by reference in their entirety.

Fabrication of embodiments of the present invention is schematically illustrated in **Figures 1A-1E**. As seen in **Figure 1A**, a substrate **10** is provided on which nitride based devices may be formed. In particular embodiments of the present invention, the substrate **10** may be a semi-insulating silicon carbide (SiC) substrate that may be, for example, 4H polytype of silicon carbide. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes. The term "semi-insulating" is used descriptively rather than in an absolute sense. In particular embodiments of the present invention, the silicon carbide bulk crystal has a resistivity equal to or higher than about $1x10^5$ Ω-cm at room temperature.

Optional buffer, nucleation and/or transition layers (not shown) may be provided on the substrate 10. For example, an AlN buffer layer may be provided to provide an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. Additionally, strain balancing transition layer(s) may also be provided as described, for example, in commonly assigned United States Patent Application Serial No. 10/199,786, filed July 19, 2002 and entitled "STRAIN BALANCED NITRIDE HETROJUNCTION TRANSISTORS AND METHODS OF FABRICATING STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTORS, and United States Provisional Patent Application Serial No. 60/337,687, filed December 3, 2001 and entitled "STRAIN BALANCED NITRIDE HETEROJUNCTION TRANSISTOR," the disclosures of which are incorporated herein by reference as if set forth fully herein.

Silicon carbide has a much closer crystal lattice match to Group III nitrides than does sapphire (Al_2O_3), which is a very common substrate material for Group III nitride devices. The closer lattice match may result in Group III nitride films of higher quality than those generally available on sapphire. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is, typically, not as limited by thermal dissipation of the substrate as in the case of the same devices formed on sapphire. Also, the availability of semi-insulating silicon carbide substrates may provide for device isolation and reduced parasitic capacitance. Appropriate SiC substrates are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and methods for producing are described, for example, in U. S. Patent Nos. Re. 34,861; 4,946,547; 5,200,022; and 6,218,680, the contents of which are incorporated herein by reference in their entirety. Similarly, techniques for epitaxial growth of Group III nitrides have been described in, for example, U. S. Patent Nos. 5,210,051; 5,393,993; 5,523,589; and 5,292,501, the contents of which are also incorporated herein by reference in their entirety.

Although silicon carbide may be the preferred substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like. In some embodiments, an appropriate buffer layer also may be formed.

Returning to Figure 1A, a channel layer 20 is provided on the substrate 10. The channel layer 20 may be deposited on the substrate 10 using buffer layers, transition layers, and/or nucleation layers as described above. The channel layer 20 may be under compressive strain. Furthermore, the channel layer and/or buffer nucleation and/or transition layers may be deposited by MOCVD or by other techniques known to those of skill in the art, such as MBE or HVPE .

In some embodiments of the present invention, the channel layer 20 is a Group III-nitride, such as $Al_xGa_{1-x}N$ where $0 \leq x < 1$, provided that the bandgap of the channel layer 20 is less than the bandgap of the first cap layer 22. In certain embodiments of the present invention, $x = 0$, indicating that the channel layer 20 is GaN. The channel layer 20 may also be other Group III-nitrides such as InGaN, AlInGaN or the like. The channel layer 20 may be undoped ("unintentionally doped") and may be grown to a thickness of greater than about 20 Å. The channel layer 20 may also be a multi-layer structure, such as a superlattice or combinations of GaN, AlGaN or the like.

A first cap layer 22 is provided on the channel layer 20. The channel layer 20 may have a bandgap that is less than the bandgap of the first cap layer 22. The first cap layer 22 may be deposited on the channel layer 20. In certain embodiments of the present invention, the first cap layer 22 is AlN, AlInN, AlGaN or AlInGaN with a thickness of between about 1 and about 10 nm. Examples of cap layers according to certain embodiments of the present invention are described in United States Patent Application Serial No. 10/102,272, to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. In particular embodiments of the present invention, the first cap layer 22 is thick enough and has a high enough Al composition and doping to induce a significant carrier concentration at the interface between the channel layer 20 and the first cap layer 22 through polarization effects when the first cap layer 22 is buried under ohmic contact metal. Also, the first cap layer 22 should be thick enough to reduce or minimize scattering of electrons in the channel due to ionized impurities deposited at the interface between the first cap layer 22 and a second cap layer 24.

The first cap layer 22 may be a Group III-nitride and has a bandgap larger than that of the channel layer 20. Accordingly, in certain embodiments of the present invention, the first cap layer 22 is AlGaN, AlInGaN and/or AlN or combinations of layers thereof. The first cap layer 22 may, for example, be from about 1 to about 10 nm thick, but is not so thick as to cause cracking or substantial defect formation therein. Preferably, the first cap layer 22 is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}. In some embodiments of the present invention, the first cap layer 22 is $Al_xGa_{1-x}N$ where $0 < x < 1$. In such embodiments, the first cap layer 22 may be from about 3 to about 15 nm thick. In particular embodiments, the aluminum concentration is about 25%. However, in other embodiments of the present invention, the first cap layer 22 comprises AlGaN with an aluminum concentration of between about 5% and about 100%. In specific embodiments of the present invention, the aluminum concentration is greater than about 10%. In embodiments of the present invention where the first cap layer 22 comprises an AlN layer, the thickness of the first cap layer 22 may, for example, be from about 0.3 nm to about 4 nm.

Figure 1B illustrates formation of a mask 30 on the first cap layer 22. The mask 30 is formed on regions of the first cap layer 22 on which ohmic contacts will subsequently be formed. In certain embodiments of the present invention, the mask 30 is slightly smaller than a size of the contact to be formed on the region of the first cap layer 22 corresponding to the mask 30 to allow for overlap of the ohmic contacts onto the additional layers to compensate for variations in alignment.

As illustrated in **Figure 1B**, the wafer of **Figure 1A** may be removed from the epi reactor and patterned with a mask material 30 over the desired recess areas. The mask material 30 should be able to withstand the growth temperature of subsequent processing, including the formation of a second cap layer 24 as described below. In certain embodiments of the present invention, the mask 30 is patterned using lift-off techniques to reduce or minimize damage or residue on the top of the first cap layer 22. Alternatively, a wet etch could be utilized to pattern the mask 30. A wet etch may be preferable for patterning over a dry etch to reduce damage to the top of the first cap layer 22. In some embodiments, the mask material 30 is removable with a wet etch that is highly selective relative to the first cap layer 22 and subsequently formed layers. In certain embodiments of the present invention, SiOx is the mask material, although other materials, such as AlN and SiNx based materials, may also be used.

The use of AlN based materials as the mask material may improve stability and reduce n-type doping from silicon and oxygen of the SiOx. If AlNx is used, it should be of such quality that it can be removed with selective wet etches.

As illustrated in **Figure 1C**, after formation and patterning of the mask **30** so as to leave the mask material in the regions where recesses are to be formed for the ohmic contacts, a second cap layer **24** is formed on the exposed regions of the first cap layer **22**. For example, the wafer of **Figure 1B** may be put back into the epi reactor for deposition of the second cap layer **24**. The first cap layer **22** and the second cap layer **24** may be the same or different materials and have the same or different compositions. For example, the first cap layer **22** may be AlN and the second cap layer **24** may be AlGaN or GaN. Furthermore, the first cap layer **22** and the second cap layer **24** may be AlGaN with a higher concentration of Al in the first cap layer **22** than in the second cap layer **24**. The total thickness of the first cap layer **22** and the second cap layer **24** may be about 25 nm. The thickness of the first cap layer **22** and the second cap layer **24** together should be thick enough and have enough Al to obtain the desired electron density but not so thick or high enough Al so as to cause cracking or substantial dislocation formation.

Alternatively, selective growth of the second cap layer **24** may be provided by providing a layer on which the material of the second cap layer **24** does not form during the growth/deposition process. For example, a mask could be a thin layer that may be removed by reactive ion etching (RIE). Alternatively, the mask may be a conductive material, such as a metal or other conductive material, such as TaN or TiN, upon which an ohmic contact may be subsequently formed and, therefore, removal of the mask may be unnecessary. In other embodiments, the mask may be formed at an area in which a gate is to be formed, and may comprise an insulating material that may be left (or only partially removed) and used as a gate insulating layer upon which a gate contact is formed.

The pre-patterned regrowth of the second cap layer **24** may also limit cracking in the regions of the second cap layer **24** in the gate/channel regions as the dimension of deposition across the channel/gate regions may be relatively small in comparison to a blanket deposition of the second cap material. In particular, the layers may have a length across the gate/channel regions (e.g., the distance between the masks **30**) on the order of a few microns (e.g., about 0.2 to about 10 microns) and a width of up to several hundred microns (e.g., about 10 microns to about 500 microns). In certain

embodiments of the present invention, the shape, dimensions, and/or crystallographic orientation of the pattern for the regrowth of the second cap layer 24 are selected to increase or maximize the allowable thickness and Al composition and, therefore, carrier concentration. The region of the second cap layer 24 may be made smaller than the typical crack spacing for a given blanket cap layer to reduce or prevent any cracking within the patterned region. Also, in some embodiments, the orientation should be such that terminating edges of the region are not orthogonal to the preferred crack directions of the crystal to minimize nucleation of cracks as they prefer to start orthogonal to the edges. Furthermore, in certain embodiments of the present invention, the second cap layer 24 has an Al composition below a level at which a substantial second electron channel forms at the regrowth interface between the first cap layer 22 and the second cap layer 24.

Growth conditions for the second cap layer 24 may be chosen to prevent excessive decomposition of mask 30. Also, any deposition on mask 30 is preferably discontinuous enough to allow for wet etching to effectively remove the mask 30 and any deposition above. Preferably, deposition is not selective so the composition of the material of the second cap layer 24, such as an AlGaN composition, and thickness are uniform over the region. A uniform composition and thickness may be achieved by using relatively low growth temperatures and/or more stable masks upon which III-nitrides nucleate (*e.g.* low quality AlNx vs. SiOx). However, nucleation should not be so complete so as to form a continuous layer on the mask 30 so as to facilitate removal of the mask 30. If the growth is selective, then the mask 30 should be sized to reduce and/or limit transport from the mask region to the growth region.

Figure 1D illustrates the formation of additional layers 26. The additional layers 26 may be deposited either in the epi reactor or externally. Because the ohmic contact regions are already going to be opened, such additional layers 26 may include GaN cap layers, as for example, described in Yu et al., "Schottky barrier engineering in III–V nitrides via the piezoelectric effect," Applied Physics Letters, Vol. 73, No. 13, 1998, or in U.S. Application Serial No. 09/904,333 filed July 12, 2001 for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," the disclosures of which are incorporated herein by reference as if set forth fully herein. In some embodiments, insulating layers such as SiNx, or relatively high

quality AlN may be deposited for making a MISHEMT, passivating the surface, and/or encapsulating the second cap layer 24 during future processing. The additional layers 26 may also include a compositionally graded transition layer on the first and/or second cap layers 22 and/or 24. The additional layers 26 may be deposited in the epi reactor directly after formation of the second cap layer 24 which may allow for improved control of the interface and surface states between the second cap layer 24 and the additional layers 26. Furthermore, because the region of the additional layers 26 has the same smaller region patterning as the second cap layer 24, these layers may also benefit from reduced cracking even if the tensile strain is increased by the additional layers 26.

Figure 1E illustrates removal of the mask 30 and formation of the ohmic contacts 40 in the recesses defined by (i.e., adjacent) the second cap layer 24. The ohmic contacts 40 may be fabricated as described in U.S. Patent No. 6,316,793. The ohmic contacts 40 are formed on the first cap layer 22. The ohmic contacts 40 on the first cap layer 22 may be annealed at a relatively low anneal temperature. For example, in certain embodiments of the present invention, anneal temperatures of from about 400 to about 800 °C may be used. In other embodiments of the present invention the anneal step may be eliminated. Thus, the ohmic contacts 40 may be provided without the need for high anneal temperatures or to etch the Group III-nitride materials of a cap layer. The transistor may be further completed by addition of a gate 28 and/or gate structure, passivation or other such additional processing as known to those of skill in the art.

The first and/or second cap layer(s) 22 and 24 may also be provided with multiple layers as described in United States Patent Application Serial No. 10/102,272, to Smorchkova *et al.*, entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosure of which is incorporated herein by reference as if set forth fully herein. Thus, embodiments of the present invention should not be construed as limiting the first and/or second cap layers to a single layer but may include, for example, barrier layers having combinations of GaN, AlGaN and/or AlN layers. For example, a GaN, AlN structure may be utilized to reduce or prevent alloy scattering. Thus, embodiments of the present invention may include nitride based barrier layers, such nitride based barrier layers may include AlGaN based barrier layers, AlN based barrier layers and combinations thereof.

Optionally, the ohmic regions may be implanted with an n-type dopant such as Si to further reduce contact resistance. If done before the regrowth, the regrowth could serve as the anneal step and/or a higher temperature anneal could be done before the last regrowth layer is deposited so that the final surface would not be affected by the high temperature anneal. For example, the first cap layer 22 may be formed of a thin AlGaN and a mask deposited and patterned to provide an implant mask with openings over the ohmic contact regions and to add alignment marks. A dopant, such as Si (or O, Ge, etc.) is implanted and the implant mask removed. The regrowth mask is then deposited and patterned to cover the ohmic contact regions and the alignment marks. The resulting structure may be annealed (~1100 °C in inert or NH_3 based gas) and an AlGaN layer formed. The regrowth mask is removed and the ohmic contacts formed.

Figure 2 illustrates an exemplary transistor according to some embodiments of the present invention. As seen in **Figure 2**, an AlN buffer layer 12 is formed on a high purity semi-insulating (HPSI) 4H SiC substrate 10'. The buffer layer 12 may be intrinsic or undoped AlN that is about 0.2 μm and the substrate 10' may be about 400 μm thick. The channel layer 20' is on the buffer layer 12 and may be an undoped GaN layer having a thickness of about 2 μm. The first cap layer 22' is on the channel layer 20' and may be an undoped AlGaN layer with an Al concentration of about 25% and a thickness of about 5 nm.

The second cap layer 24' is selectively grown utilizing a mask as described above as a doped AlGaN layer, intentionally or otherwise, with an Al concentration of about 20% and doped with an n-type dopant such as Si to a concentration of about 2 X 10^{12} cm^{-2} total. The second cap layer 24' may have a thickness of about 10 nm. An additional layer 26' is selectively grown utilizing a mask as described above as an undoped AlGaN with an Al concentration of about 20% is also provided on the second cap layer 24'. The additional layer 26' may have a thickness of about 10 nm. Ohmic contacts 40 are formed in the recesses adjacent the second cap layer 24' and the additional layer 26'. A gate contact 28' may be formed on the additional layer 26'.

Figure 3 illustrates an exemplary transistor according to some embodiments of the present invention utilizing an AlN barrier layer. As seen in **Figure 3**, the substrate, the AlN buffer layer 12 and the channel layer 20' may be provided as described above with reference to **Figure 2**. The first cap layer 22'' is on the channel layer 20' and may be an undoped AlN layer having a thickness of about 1nm.

The second cap layer 24'' is selectively grown utilizing a mask as described above as an undoped AlGaN layer with an Al concentration of about 20%. The second cap layer 24'' may have a thickness of about 20 nm. Ohmic contacts 40 are formed in the recesses adjacent the second cap layer 24''. A gate contact 28'' may be formed on the second cap layer 24''.

Figure 4 illustrates an exemplary transistor according to some embodiments of the present invention where the selective regrowth is utilized to provide a recessed gate structure. As seen in Figure 4, the substrate, the AlN buffer layer 12 and the channel layer 20' may be provided as described above with reference to Figure 2. The first cap layer 22''' is on the channel layer 20' and may be an undoped AlGaN layer with an Al concentration of about 25% and a thickness of up to about 25 nm.

The second cap layer 24''' is selectively grown utilizing a mask as described above except the mask is used to mask the gate region of the device. The second cap layer 24''' may be an undoped AlGaN layer with an Al concentration of about 20%. The second cap layer 24''' may have a thickness of about 5 nm. An additional layer 26'' is selectively grown utilizing a mask as described above as a doped AlGaN layer doped n+, for example, doped to a carrier concentration of from about 10^{18} to about 10^{20} cm^{-3}. The additional layer 26'' may have an Al concentration of about 20%. The additional layer 26'' may have a thickness of about 10 nm. Ohmic contacts 40' are formed on the additional layer 26''. A gate contact 42 may be formed on the first cap layer 22''' in the recess formed by the second cap layer 24''' and the additional layer 26''.

Figure 5 shows a transistor according to further exemplary embodiments of the present invention, in which gate and ohmic contacts are both formed in regrown recesses. A channel layer 520 and a first cap layer 522 may be formed on a substrate 510 as described above (it will be appreciated that the substrate 510 may include buffer layers and/or other layers). The first cap layer 522 may be masked to expose portions of the first cap layer 522, and second cap layers 524 may be formed on the exposed portions. The mask may then be removed to leave recesses adjacent the second cap layers 524. Ohmic and gate contacts 540 and 528 may be formed in the recesses, as shown.

Figure 6 shows a transistor according to other exemplary embodiments of the present invention, in which gate and ohmic contacts are both formed in regrown recesses, but on different nitride-based layers. A channel layer 620 and a first cap

layer 622 may be formed on a substrate 610 as described above (it will be appreciated that the substrate 610 may include buffer layers and/or other layers). The first cap layer 622 may be masked to expose a portion of the first cap layer 622. A second cap layer 624 may then be formed on the exposed portion. An additional mask may then be formed on the second cap layer 624, leaving spaced apart portions of the second cap layer exposed. Additional layers 626 may be formed on these exposed portions. The masks may be removed to leave recesses that expose first and second portions of the first cap layer 622 and a portion of the second cap layer 624. Ohmic and gate contacts 640 and 628 may be formed in the recesses, as shown. It will be appreciated that the order of masking and contact formation operations may be varied.

In the drawings and specification, there have been disclosed typical embodiments of the invention, and, although specific terms have been employed, they have been used in a generic and descriptive sense only and not for purposes of limitation.

THAT WHICH IS CLAIMED IS:

1. A method of fabricating a transistor, the method comprising:

forming a nitride-based channel layer on a substrate;

forming a nitride-based semiconductor first cap layer on the nitride-based channel layer;

forming a mask that covers a first portion of the first cap layer and exposes an adjacent second portion of the first cap layer;

forming a nitride-based semiconductor second cap layer on the exposed second portion of the first cap layer using the mask;

forming a recess on the first portion of the first cap layer adjacent the second cap layer;

forming one of an ohmic contact or a gate contact in the recess; and

forming a corresponding gate contact or ohmic contact on the substrate.

2. A method according to Claim 1, wherein forming a corresponding gate contact or ohmic contact comprises forming the corresponding gate contact or ohmic contact on the second cap layer.

3. A method according to Claim 1:

wherein the mask comprises a conductive material;

wherein forming a recess comprises forming a recess exposing the mask; and

wherein forming one of an ohmic contact or a gate contact comprises forming one of an ohmic contact or a gate contact on the mask in the recess.

4. A method according to Claim 1:

wherein the mask comprises an insulating material;

wherein forming a recess comprises forming a recess exposing the mask; and

wherein forming one of an ohmic contact or a gate contact comprises forming a gate contact on the exposed mask.

5. A method according to Claim 1:

wherein forming a recess comprises removing the mask to expose the first portion of the first cap layer and to form a recess adjacent the second cap layer; and

wherein forming one of an ohmic contact or a gate contact comprises forming one of an ohmic contact or a gate contact on the exposed portion of the first cap layer.

6. A method according to Claim 1:

wherein forming a mask comprises forming a mask that covers spaced apart first portions of the first cap layer and that exposes a second portion of the first cap layer therebetween;

wherein forming a recess comprises removing the mask to expose the first portions of the first cap layer and to form first and second recesses adjacent the second cap layer;

wherein forming one of an ohmic contact or a gate contact comprises forming an ohmic contact in the first recess; and

wherein forming a corresponding gate contact or ohmic contact comprises forming a gate contact in the second recess.

7. A method according to Claim 1:

wherein forming a nitride-based channel layer comprises forming a Group III-nitride layer;

wherein forming a nitride-based semiconductor first cap layer comprises forming a Group III-nitride layer; and

wherein forming a nitride-based semiconductor second cap layer comprises growing a Group-III nitride layer.

8. A method according to Claim 7, wherein the channel layer has a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, and wherein the bandgap of the channel layer is less than the bandgap of the first cap layer.

9. A method according to Claim 7, wherein the channel layer comprises GaN, InGaN, and/or AlInGaN.

10. A method according to Claim 7, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

11. A method according to Claim 7, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

12. A method according to Claim 7:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN);

wherein the first cap layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN; and

wherein the second cap layer comprises aluminum nitride (AlN), AlInN, AlGaN, GaN, InGaN, and/or AlInGaN.

13. A method according to Claim 7, wherein the first cap layer comprises AlN, AlInN, AlGaN, and/or AlInGaN, and has a thickness of 1 nm to about 10 nm.

14. A method according to Claim 7, wherein the first cap layer is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}.

15. A method according to Claim 7, the first cap layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

16. A method according to Claim 15, wherein the first cap layer has a thickness of about 3 nm to about 15 nm.

17. A method according to Claim 7, wherein the first cap layer comprises AlGaN with an aluminum concentration of between about 5% and about 100%.

18. A method according to Claim 17, wherein the first cap layer has an aluminum concentration greater than about 10%.

19. A method according to Claim 7, wherein the first cap layer comprises an AlN layer having a thickness of about 0.3 nm to about 4 nm.

20. A method according to Claim 7, wherein the channel layer has a lower bandgap than the first cap layer.

21. A method according to Claim 1, wherein forming a mask comprises patterning a mask layer using one of a lift-off technique or a wet-etch technique.

22. A method according to Claim 1, wherein forming a mask comprises a forming the mask from a silicon oxide (SiOx), a silicon nitride (SiNx) or an AlN-based material.

23. A method according to Claim 1, wherein the second cap layer comprises the same material as the first cap layer.

24. A method according to Claim 23, wherein the first and second cap layers comprise AlGaN, and wherein the first cap layer has a higher concentration of Al than the second cap layer.

25. A method according to Claim 24, wherein a combined thickness of the first and second cap layers is about 25 nm.

26. A method according to Claim 1, wherein the second cap layer has an orientation such that terminating edges of the second cap layer are not orthogonal to preferred crystal crack directions.

27. A method according to Claim 1, wherein the second cap layer has an Al composition below a level at which a substantial second electron channel forms at a regrowth interface between the first cap layer and the second cap layer.

28. A method according to Claim 1, further comprising forming an additional layer on the second cap layer.

29. A method according to Claim 28, wherein the additional layer comprises at least one of a GaN cap layer, an insulating layer, and a compositionally graded transition layer.

30. A method according to Claim 1, wherein the first and second cap layer each comprise multiple layers.

31. A method according to Claim 1, wherein at least one of the first and second cap layers comprises a nitride-based barrier layer.

32. A method according to Claim 1, further comprising implanting an ohmic contact region of the first cap layer with an n-type dopant before forming the contact in the recess.

33. A method according to Claim 32, wherein implanting an ohmic contact region comprises implanting the ohmic contact region before the growth of the second cap layer.

34. A method according to Claim 1, wherein forming a nitride-based channel layer is preceded by forming a buffer layer on the substrate, and wherein forming a nitride-based channel layer comprises forming the nitride-based channel layer on the buffer layer.

35. A method according to Claim 1:

wherein forming a nitride-based channel layer is preceded by forming a buffer layer on a substrate;

wherein forming a nitride-based channel layer comprises forming a Group III-nitride channel layer on the buffer layer;

wherein forming a nitride-based semiconductor first cap layer comprises forming a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein forming a mask comprises forming a mask covering spaced-apart first portions of the first cap layer and exposing a second adjacent portion of the first cap layer between the first portions;

wherein growing a nitride-based semiconductor second cap layer comprises growing a Group III-nitride second cap layer on the exposed second portion of the first cap layer;

wherein the method further comprises forming a third semiconductor layer on the second cap layer;

wherein forming a recess comprises removing the mask to form recesses that expose the first portions of the first cap layer;

wherein forming one of an ohmic contact or a gate contact comprises forming respective ohmic contacts in the recesses; and

wherein forming a corresponding gate contact or ohmic contact comprises forming a gate contact on the third semiconductor layer.

36. A method according to Claim 35:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H silicon carbide (SiC) substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer with an Al concentration of about 25% and a thickness of about 5 nm;

wherein the second cap layer comprises an n-doped AlGaN layer with an Al concentration of about 20% , a dopant concentration of about 2 X 10^{12} cm^{-2}, and a thickness of about 10 nm; and

wherein the third semiconductor layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 10 nm.

37. A method according to Claim 35:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlN layer having a thickness of about 1 nm;

wherein the second cap layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 20 nm.

38. A method according to Claim 1:

wherein forming a nitride-based channel layer is preceded by forming a buffer layer on a substrate;

wherein forming a nitride-based channel layer comprises forming a Group III-nitride channel layer on the buffer layer;

wherein forming a nitride-based semiconductor first cap layer comprises forming a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein forming a mask comprises forming a mask covering a first portion of the first cap layer and exposing second portions of the first cap layer on opposite sides of the first portion;

wherein growing a nitride-based semiconductor second cap layer comprises growing Group III-nitride second cap layers on respective ones of the exposed second portions of the first cap layer;

wherein the method further comprises forming respective third semiconductor layers on the respective second cap layers;

wherein forming a recess comprises removing the mask to expose the first portions of the first cap layer;

wherein forming one of an ohmic contact or a gate contact comprises forming a gate contact on the exposed portion of the first cap layer; and

wherein forming a corresponding gate contact or ohmic contact comprises forming respective ohmic contacts on the third semiconductor layers.

39. A method according to Claim 38:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer having a thickness of about 25 nm and an aluminum concentration of about 25%;

wherein the second cap layers comprises undoped AlGaN layers having a thickness of about 5 nm and an aluminum concentration of about 20%;

wherein the third semiconductor layers comprise doped AlGaN layers having a thickness of about 10 nm and an aluminum concentration of about 20%.

40. A method according to Claim 1, wherein forming a nitride-based semiconductor second cap layer comprises growing the second cap layer on the exposed portion of the first cap layer.

41. A method according to Claim 1, where the channel layer and the first and second cap layers are configured to provide a High Electron Mobility Transistor (HEMT).

42. A method of fabricating a contact for a nitride-based microelectronic device, the method comprising;

forming a nitride-based semiconductor first layer on a substrate;

forming a mask that covers a first portion of the first layer and exposes an adjacent second portion of the first layer;

forming a nitride-based semiconductor second layer on the exposed portion of the first layer using the mask;

forming a recess on the first portion of the first cap layer adjacent the second layer; and

forming a contact in the recess.

43. A method according to Claim 42:

wherein the mask comprises a conductive material;

wherein forming a recess comprises forming a recess exposing the mask; and

wherein forming a contact comprises forming a contact on the mask in the recess.

44. A method according to Claim 1:

wherein forming a recess comprises removing the mask to expose the first portion of the first layer and to form a recess adjacent the second layer; and

wherein forming a contact comprises forming a contact on the exposed portion of the first layer.

45. A method according to Claim 42:

wherein forming a nitride-based semiconductor first layer comprises forming a Group III-nitride layer; and

wherein forming a nitride-based semiconductor second layer comprises growing a Group-III nitride layer.

46. A method according to Claim 42, wherein forming a nitride-based semiconductor second layer comprises growing the second layer on the exposed first portion of the first layer.

47. A transistor, comprising:

a nitride-based channel layer on a substrate;

a nitride-based semiconductor first cap layer on the nitride-based channel layer;

a grown nitride-based semiconductor second cap layer on the first cap layer;

an ohmic contact or a gate contact disposed directly on the first cap layer, adjacent a sidewall of the grown second cap layer; and

a corresponding gate contact or ohmic contact on the substrate.

48. A transistor according to Claim 47, wherein the corresponding gate contact or ohmic contact is on the second cap layer.

49. A transistor according to Claim 46:

wherein the ohmic contact or gate contact disposed directly on the first cap layer comprises an ohmic contact disposed directly on the first cap layer; and

wherein the corresponding gate contact or ohmic contact comprises a gate contact directly on the first cap layer.

50. A transistor according to Claim 47:

wherein the nitride-based channel layer comprises a Group III-nitride layer;

wherein the nitride-based semiconductor first cap layer comprises a Group III-nitride layer; and

wherein the grown nitride-based semiconductor second cap layer comprises a grown Group-III nitride layer.

51. A method according to Claim 50, wherein the channel layer has a composition of $Al_xGa_{1-x}N$ wherein $0 \leq x < 1$, and wherein the bandgap of the channel layer is less than the bandgap of the first cap layer.

52. A transistor according to Claim 49, wherein the channel layer comprises GaN, InGaN, and/or AlInGaN.

53. A transistor according to Claim 50, wherein the channel layer comprises an undoped layer having a thickness of greater than about 20 Å.

54. A transistor according to Claim 50, wherein the channel layer comprises a superlattice and/or a combination of Group III-nitride layers.

55. A transistor according to Claim 50:

wherein the channel layer comprises aluminum gallium nitride (AlGaN), gallium nitride (GaN), indium gallium nitride (InGaN), and/or aluminum indium gallium nitride (AlInGaN);

wherein the first cap layer comprises aluminum nitride (AlN), aluminum indium nitride (AlInN), AlGaN, GaN, InGaN, and/or AlInGaN; and

wherein the second cap layer comprises aluminum nitride (AlN), AlInN, AlGaN, GaN, InGaN, and/or AlInGaN.

56. A transistor according to Claim 50, wherein the first cap layer comprises AlN, AlInN, AlGaN, and/or AlInGaN, and has a thickness of 1 nm to about 10 nm.

57. A transistor according to Claim 50, wherein the first cap layer is undoped or doped with an n-type dopant to a concentration less than about 10^{19} cm^{-3}.

58. A transistor according to Claim 50, the first cap layer comprises $Al_xGa_{1-x}N$ wherein $0 < x < 1$.

59. A transistor according to Claim 58, wherein the first cap layer has a thickness of about 3 nm to about 15 nm.

60. A transistor according to Claim 50, wherein the first cap layer comprises AlGaN with an aluminum concentration of between about 5% and about 100%.

61. A transistor according to Claim 60, wherein the first cap layer has an aluminum concentration greater than about 10%.

62. A transistor according to Claim 50, wherein the first cap layer comprises an AlN layer having a thickness of about 0.3 nm to about 4 nm.

63. A transistor according to Claim 50, wherein the channel layer has a lower bandgap than the first cap layer.

64. A transistor according to Claim 47, wherein the second cap layer comprises the same material as the first cap layer.

65. A transistor according to Claim 64, wherein the first and second cap layers comprise AlGaN, and wherein the first cap layer has a higher concentration of Al than the second cap layer.

66. A transistor according to Claim 65, wherein a combined thickness of the first and second cap layers is about 25 nm.

67. A transistor according to Claim 47, wherein the second cap layer has an orientation such that terminating edges of the second cap layer are not orthogonal to a preferred crystal crack direction.

68. A transistor according to Claim 47, wherein the second cap layer has an Al composition below a level at which a substantial second electron channel forms at a regrowth interface between the first cap layer and the second cap layer.

69. A transistor according to Claim 47, further comprising an additional layer on the second cap layer.

70. A transistor according to Claim 69, wherein the additional layer comprises at least one of a GaN cap layer, an insulating layer, and a compositionally graded transition layer.

71. A transistor according to Claim 47, wherein the first and second cap layers each comprise multiple layers.

72. A transistor according to Claim 47, wherein at least one of the first and second cap layers comprises a nitride-based barrier layer.

73. A transistor according to Claim 47, further comprising a buffer layer on the substrate, and wherein the nitride-based channel layer is disposed on the buffer layer.

74. A transistor according to Claim 47:

wherein the nitride-based channel layer comprises a Group III-nitride channel layer on a buffer layer;

wherein the nitride-based semiconductor first cap layer comprises a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein the grown nitride-based semiconductor second cap layer comprises a grown Group III-nitride second cap layer on the exposed second portion of the first cap layer;

wherein the transistor further comprises a third semiconductor layer on the second cap layer;

wherein an ohmic contact or a gate contact comprises respective ohmic contacts adjacent opposite sidewalls of the second cap layer; and

wherein the corresponding gate contact or ohmic contact comprises a gate contact on the third semiconductor layer.

75. A transistor according to Claim 74:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H silicon carbide (SiC) substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer with an Al concentration of about 25% and a thickness of about 5 nm;

wherein the second cap layer comprises an n-doped AlGaN layer with an Al concentration of about 20% , a dopant concentration of about 2×10^{12} cm^{-2}, and a thickness of about 10 nm; and

wherein the third semiconductor layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 10 nm.

76. A transistor according to Claim 74:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlN layer having a thickness of about 1 nm;

wherein the second cap layer comprises an undoped AlGaN layer with an Al concentration of about 20% and a thickness of about 20 nm.

77. A transistor according to Claim 47:

wherein the nitride-based channel layer comprises a Group III-nitride channel layer on a buffer layer;

wherein the nitride-based semiconductor first cap layer a Group III-nitride first cap layer on the channel layer, the first cap layer having a bandgap greater than the channel layer;

wherein the grown nitride-based semiconductor second cap layer comprises grown Group III-nitride second cap layers on respective spaced apart portions of the first cap layer;

wherein the transistor comprises forming respective third semiconductor layers on the respective second cap layers;

wherein an ohmic contact or a gate contact comprises a gate contact on a portion of the first cap layer between the second cap layers; and

wherein a corresponding gate contact or ohmic contact comprises respective ohmic contacts on the third semiconductor layers.

78. A transistor according to Claim 77:

wherein the substrate comprises a high purity semi-insulating (HPSI) 4H SiC substrate having a thickness of about 400 μm ;

wherein the buffer layer comprises an intrinsic or undoped AlN layer having a thickness of about 0.2 μm;

wherein the channel layer comprises an undoped GaN layer having a thickness of about 2 μm;

wherein the first cap layer comprises an undoped AlGaN layer having a thickness of about 25 nm and an aluminum concentration of about 25%;

wherein the second cap layers comprises undoped AlGaN layers having a thickness of about 5 nm and an aluminum concentration of about 20%;

wherein the third semiconductor layers comprise doped AlGaN layers having a thickness of about 10 nm and an aluminum concentration of about 20%.

79. A transistor according to Claim 47, wherein the channel layer and the first and second cap layers are configured to provide an HEMT.

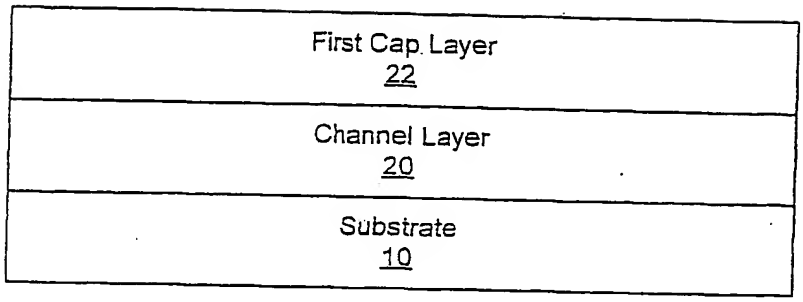

Figure 1A

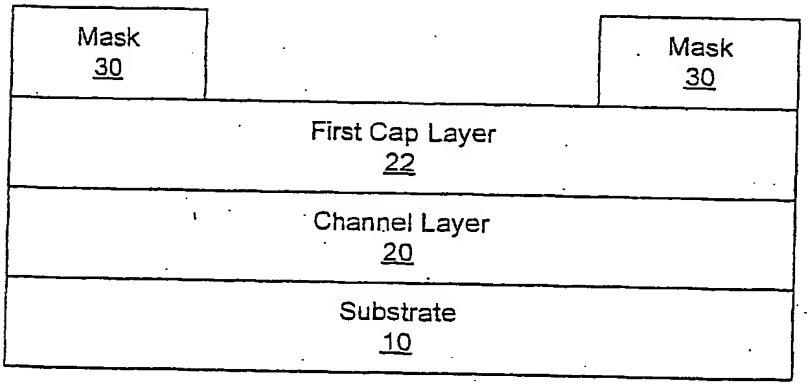

Figure 1B

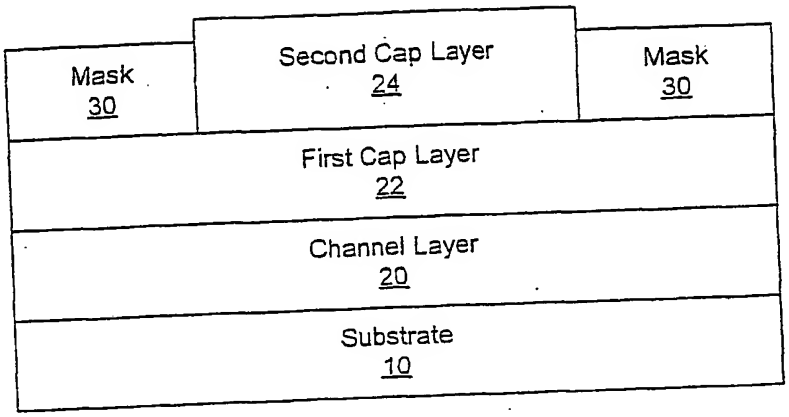

Figure 1C

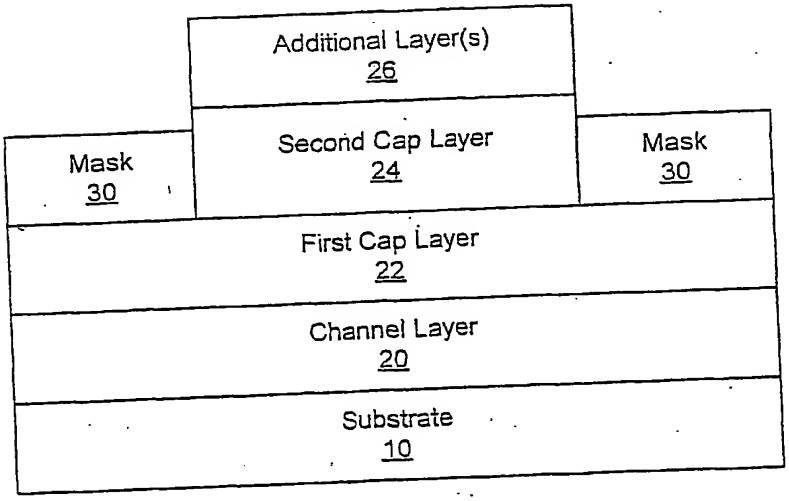

Figure 1D

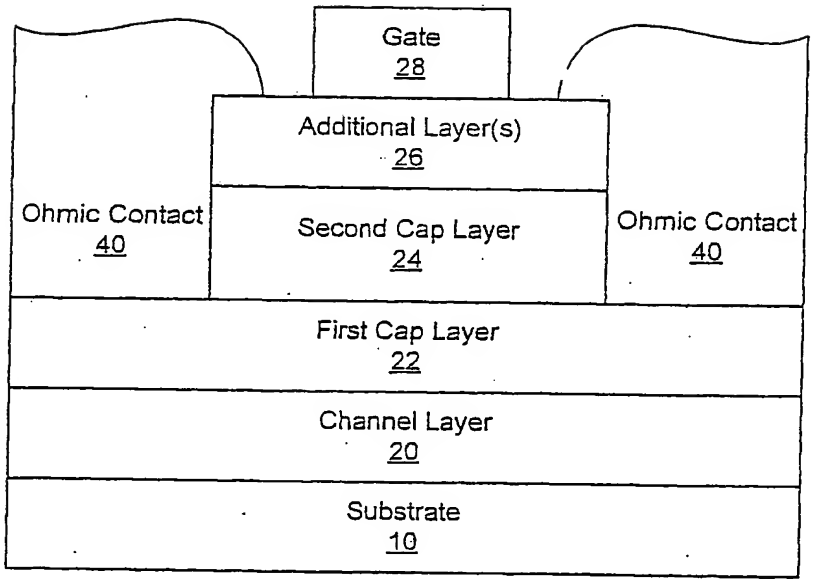

Figure 1E

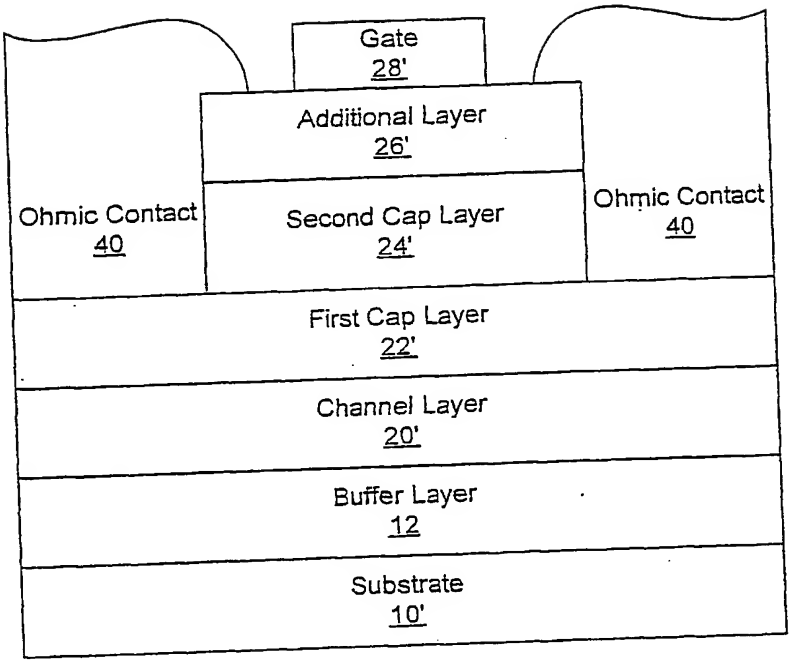
Gate
28'
Additional Layer
26'
Ohmic Contact
40
Second Cap Layer
24'
Ohmic Contact
40
First Cap Layer
22'
Channel Layer
20'
Buffer Layer
12
Substrate
10'

Figure 2

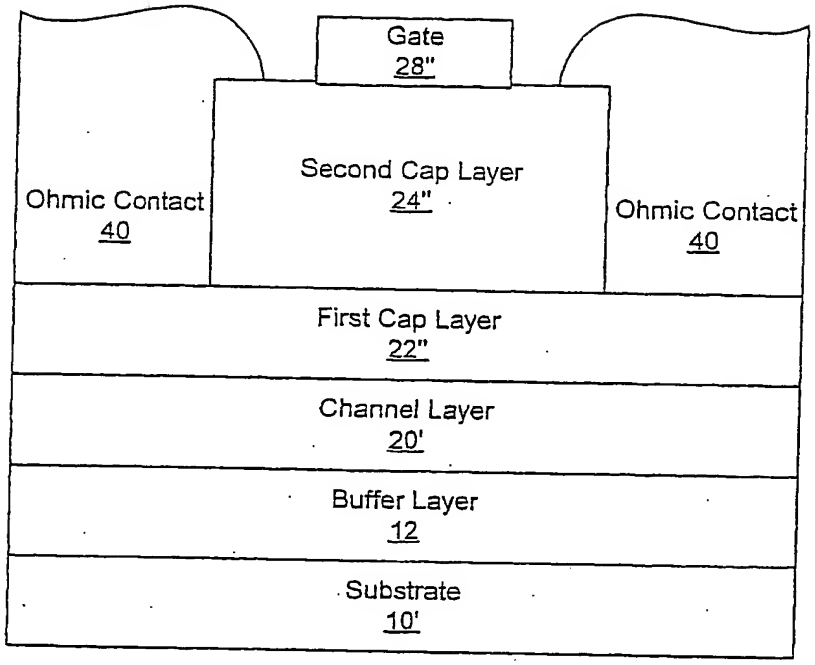

Figure 3

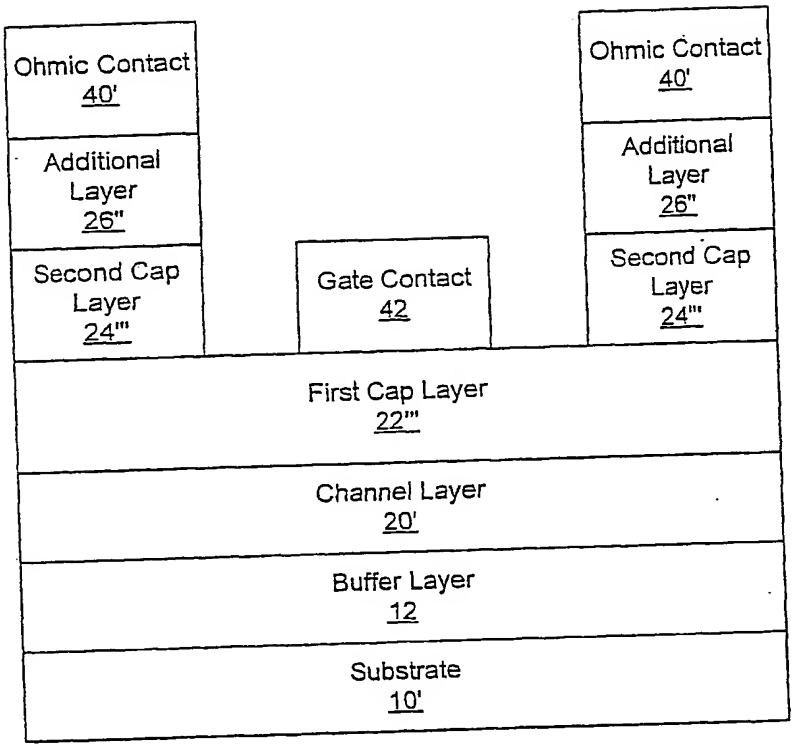
Ohmic Contact
40'
Additional
Layer
26"
Second Cap
Layer
24'''
Gate Contact
42
Ohmic Contact
40'
Additional
Layer
26"
Second Cap
Layer
24'''
First Cap Layer
22'''
Channel Layer
20'
Buffer Layer
12
Substrate
10'

Figure 4

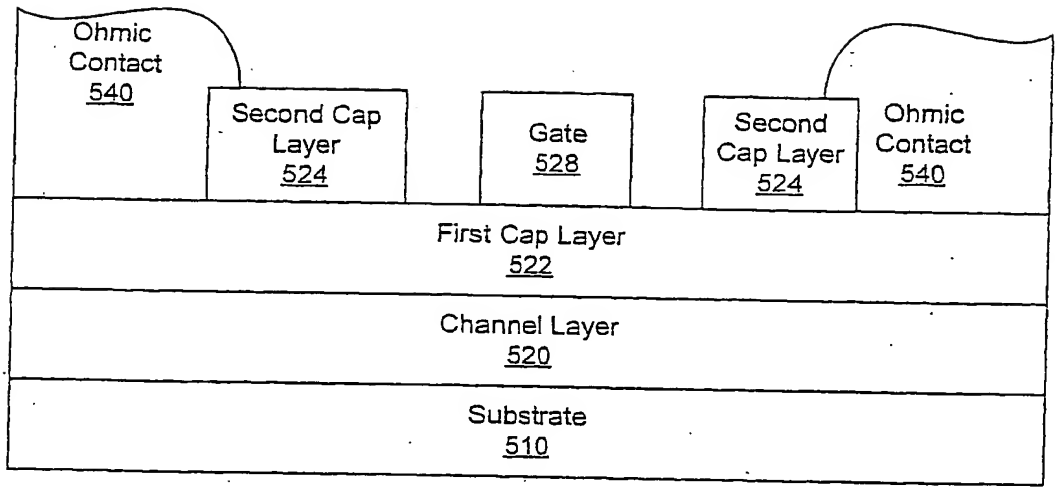

Figure 5

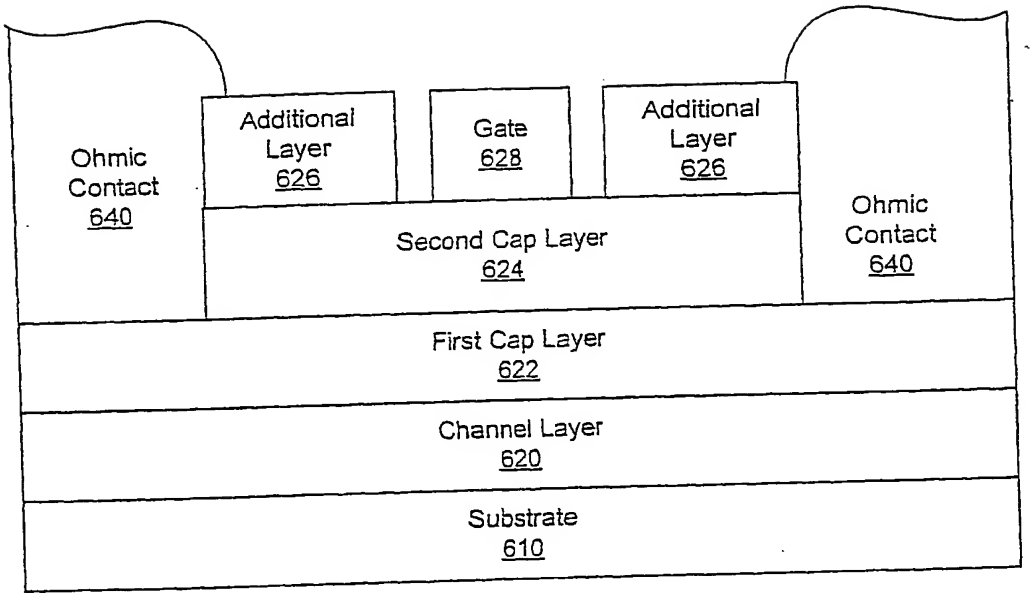
Ohmic Contact 640
Additional Layer 626
Gate 628
Additional Layer 626
Ohmic Contact 640
Second Cap Layer 624
First Cap Layer 622
Channel Layer 620
Substrate 610

Figure 6

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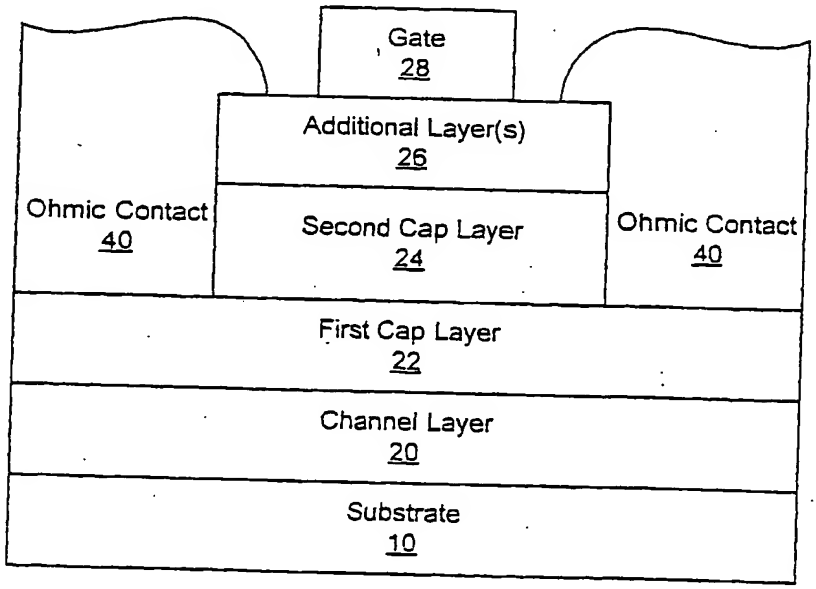
(54) Title: NITRIDE-BASED TRANSISTORS AND METHODS OF FABRICATION THEREOF USING NON-ETCHED CONTACT RECESSES



(57) Abstract: Contacts for a nitride based transistor and methods of fabricating such contacts provide a recess through a regrowth process. The contacts are formed in the recess. The regrowth process includes fabricating a first cap layer comprising a Group III-nitride semiconductor material. A mask is fabricated and patterned on the first cap layer. The pattern of the mask corresponds to the pattern of the recesses for the contacts. A second cap layer comprising a Group III-nitride semiconductor material is selectively fabricated (e.g. grown) on the first cap layer utilizing the patterned mask. Additional layers may also be formed on the second cap layer. The mask may be removed to provide recess(es) to the first cap layer, and contact(s) may be formed in the recess(es). Alternatively, the mask may comprise a conductive material upon which a contact may be formed, and may not require removal.

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International Application No
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5 298 445 A (ASANO KAZUNORI) 29 March 1994 (1994-03-29) the whole document	1-46
A	US 6 316 793 B1 (PALMOUR JOHN WILLIAMS ET AL) 13 November 2001 (2001-11-13) cited in the application the whole document	1-79

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
1 December 2003	09/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Baillet, B

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INTERNATIONAL SEARCH REPORT

Int onal Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	EGAWA T ET AL: "CHARACTERIZATIONS OF RECESSED GATE ALGAN/GAN HEMTS ON SAPPHIRE" IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE INC. NEW YORK, US, vol. 48, no. 3, March 2001 (2001-03), pages 603-608, XP001039005 ISSN: 0018-9383 the whole document	1-79
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